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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/670,908	09/25/2003	Robert Allen	16356.820 (DC-05171)	6511

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EXAMINER	
SUN, XIUQIN	
ART UNIT	**PAPER NUMBER**
2863	

DATE MAILED: 01/21/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/670,908	ALLEN ET AL.	
	Examiner	Art Unit	
	Xiuqin Sun	2863	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 September 2003 and 16 August 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,14-18 and 23-25* is/are rejected.

7)☒ Claim(s) *5-13 and 19-22* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *25 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-3 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Takamisawa et al. (U.S. Pat. No. 4357574) in view of Cantwell et al. (U.S. Pub. No. 20040215953).

Takamisawa et al. teach a method of testing a power supply in a unit under test, comprising: activating a diagnostic test circuit in the power supply for a first time period (col. 4, lines 54-67; col. 5, lines 1-17; col. 7, lines 41-67 and col. 8, lines 1-15); and supplying power, by the power supply, to a test load resistor in the power supply for a second time period within the first time period, the second time period being controlled by the diagnostic test circuit (col. 3, lines 1-55; col. 5, lines 33-46; col. 7, lines 41-67 and col. 8, lines 1-15). The teaching of Takamisawa et al. further includes: said second time period is sufficiently short to prevent overheating of the test load resistor (col. 3, lines 1-55); and inactivating the diagnostic test circuit after the first time period has expired (col. 4, lines 54-67; col. 5, lines 1-17; col. 7, lines 41-67 and col. 8, lines 1-15).

Takamisawa et al. do not mention explicitly: applying said method to an information handling system; and said test is initiated by a customer in response to an instruction received from a call center from which service is requested

Cantwell et al. teach a method of operating an information handling system (IHS), including the step of testing a power supply in said HIS (sections 0012 and 0021). The teaching of Cantwell further includes the limitation that: test can be initiated by a customer in response to an instruction received from a call center from which service is requested (sections 0019-0021).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to combine the teaching of Cantwell et al. with the invention of Takamisawa in order to provide an effective method for testing a power supply in a HIS (Cantwell et al., section 0012). The mere application of a known technique to a specific instance by those skilled in the art would have been obvious.

3. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Takamisawa et al. (U.S. Pat. No. 4357574) in view of Cantwell et al. (U.S. Pub. No. 20040215953), as applied to claim 1 above, and further in view of Conroy (U.S. Pat. No. 4414601).

Takamisawa et al. and Cantwell et al. teach the method that includes the subject matter discussed above. The combination of Takamisawa and Cantwell does not mention: delaying the supplying of power to the test load resistor for the duration of a cool down time delay period to allow the test load resistor to cool.

Conroy teaches a solid state load protection system whereby the current supplied to a load is monitored enabling a test feature to be used, including the means of delaying the supplying of power to the test load resistor for the duration of a cool down time delay period to allow the test load resistor to cool (col. 8, lines 27-37; col. 9, lines 1-6; col. 12, lines 54-67; col. 13, lines 1-12; col. 16, lines 60-67 and col. 17, lines 1-15).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to include the teaching of Conroy into the combination of Takamisawa and Cantwell in order to enable the test load resistor to cool down after an overheating condition (Conroy, col. 16, lines 60-67 and col. 17, lines 1-15).

4. Claims 15-17, 23 and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Takamisawa et al. (U.S. Pat. No. 4357574) in view of Cantwell et al. (U.S. Pub. No. 20040215953).

Takamisawa et al. teach a system comprising: a power supply for supplying power to a system board (col. 2, lines 58-67 and col. 3, lines 1-55), the power supply including: a diagnostic test actuation mechanism (col. 3, lines 1-55; col. 4, lines 55-67; col. 5, lines 1-17 and lines 33-46); a diagnostic test circuit which in response to actuation of the test actuation mechanism is activated for a first time period (col. 3, lines 1-55; col. 4, lines 55-67; col. 5, lines 1-17 and lines 33-46; col. 7, lines 41-67 and col. 8, lines 1-17); and a test load resistor to which power is supplied by the power supply for a second time period within the first time period, the second time period being controlled by the diagnostic test circuit (col. 3, lines 1-55; col. 4, lines 55-67; col. 5, lines 1-17 and

lines 33-46; col. 7, lines 41-67 and col. 8, lines 1-17). The teaching of Takamisawa et al. further includes: said second time period is sufficiently short to prevent overheating of the test load resistor (col. 3, lines 1-55); and inactivating the diagnostic test circuit after the first time period has expired (col. 4, lines 54-67; col. 5, lines 1-17; col. 7, lines 41-67 and col. 8, lines 1-17).

Takamisawa et al. do not mention explicitly: said system is an information handling system (IHS); said system board includes a processor; a diagnostic test actuation mechanism is a switch which can be activated by a user; and said diagnostic test actuation mechanism is an AC power detector.

Cantwell et al. teach a method of testing power supply in an information handling system (IHS) (sections 0012 and 0021), including a system board contains a processor (section 0019). The teaching of Cantwell et al. further includes: a diagnostic test actuation mechanism is a switch which can be activated by a user (sections 0018-0021); and said diagnostic test actuation mechanism is an AC power detector (sections 0018-0021).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to combine the teaching of Cantwell et al. with the invention of Takamisawa in order to provide an effective system for testing a power supply in a HIS (Cantwell et al., section 0012). The mere application of a known technique to a specific instance by those skilled in the art would have been obvious.

5. Claim 18 is rejected under 35 U.S.C. 103(a) as being unpatentable over Takamisawa et al. (U.S. Pat. No. 4357574) in view of Cantwell et al. (U.S. Pub. No.

20040215953), as applied to claim 15 above, and further in view of Conroy (U.S. Pat. No. 4414601).

Takamisawa et al. and Cantwell et al. teach the system that includes the subject matter discussed above. The combination of Takamisawa and Cantwell does not mention: the supplying of power to the test load resistor is delayed for the duration of a cool down time delay period to allow the test load resistor to cool.

Conroy teaches a solid state load protection system whereby the current supplied to a load is monitored enabling a test feature to be used, including the means of delaying the supplying of power to the test load resistor for the duration of a cool down time delay period to allow the test load resistor to cool (col. 8, lines 27-37; col. 9, lines 1-6; col. 12, lines 54-67; col. 13, lines 1-12; col. 16, lines 60-67 and col. 17, lines 1-15).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to include the teaching of Conroy into the combination of Takamisawa and Cantwell in order to enable the test load resistor to cool down after an overheating condition (Conroy, col. 16, lines 60-67 and col. 17, lines 1-15).

6. Claim 25 is rejected under 35 U.S.C. 103(a) as being unpatentable over Takamisawa et al. (U.S. Pat. No. 4357574) in view of Cantwell et al. (U.S. Pub. No. 20040215953).

Takamisawa et al. teach a system of testing a power supply in a unit under test, comprising: a chassis (col. 8, lines 50-65), a power supply for supplying power to a system board (col. 2, lines 58-67 and col. 3, lines 1-55), the power supply including: a

diagnostic test actuation mechanism (col. 3, lines 1-55; col. 4, lines 55-67; col. 5, lines 1-17 and lines 33-46; col. 7, lines 41-67 and col. 8, lines 1-17); a diagnostic test circuit which in response to actuation of the test actuation mechanism is activated for a first time period (col. 3, lines 1-55; col. 4, lines 55-67; col. 5, lines 1-17 and lines 33-46; col. 7, lines 41-67 and col. 8, lines 1-17); and a test Load resistor to which power is supplied by the power supply for a second time period within the first time period, the second time period being controlled by the diagnostic test circuit (col. 3, lines 1-55; col. 4, lines 55-67; col. 5, lines 1-17 and lines 33-46; col. 7, lines 41-67 and col. 8, lines 1-17).

Takamisawa et al. do not mention explicitly: said system is an information handling system (HIS), including: a microprocessor mounted on a system board in the chassis; and a storage coupled to the microprocessor.

Cantwell et al. teach a method of testing power supply in an information handling system (IHS) (sections 0012 and 0021), including a system board contains a microprocessor and a storage coupled to the microprocessor (section 0019).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to combine the teaching of Cantwell et al. with the invention of Takamisawa in order to provide an effective system for testing a power supply in a HIS (Cantwell et al., section 0012). The mere application of a known technique to a specific instance by those skilled in the art would have been obvious.

Allowable Subject Matter

7. Claims 5-13 and 19-22 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Reasons for Allowance

8. The following is an examiner's statement of reasons for allowance:

The primary reason for the allowance of claims 5-13 is the inclusion of the claimed method step of monitoring a power good signal from a housekeeping controller which monitors voltages within the power supply. It is this limitation found in each of the claims, as it is claimed in the combination that has not been found, taught or suggested by the prior art of record, which makes these claims allowable over the prior art.

The primary reason for the allowance of claims 19-22 is the inclusion of the limitation of a housekeeping controller for monitoring voltages within the power supply to provide a power good signal. It is this limitation found in each of the claims, as it is claimed in the combination that has not been found, taught or suggested by the prior art of record, which makes these claims allowable over the prior art.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Prior Art Citations

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

1) Arsenault et al. (U.S. Pat. No. 6396256) is entitled to "Power supply slew time testing of electronic circuits".

2) Sparkman (U.S. Pub. No. 20040130334) is entitled to "Timing markers used in the measurement and testing of a printed circuit board's controlled impedance".

3) Hopkins et al. (U.S. Pat. No. 6366208) is entitled to "Diagnostic functions for power supply"

Contact Information

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Xiuqin Sun whose telephone number is (571)272-2280. The examiner can normally be reached on 6:30am-4:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Barlow can be reached on (571)272-2269. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only.

For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Xiuqin Sun
Examiner
Art Unit 2863

XS
January 5, 2005

John Barlow
Supervisory Patent Examiner
Technology Center 2800